

# Improvement of Photoresist Film Coverage on High Topology Surface with Spray Coating Technique

Nithi Atthi, Karoon Saejok, Jakrapong Supadech, Wutthinan Jeamsaksiri, Oraphan Thongsuk,

Paweena Dulyaseree, Charndet Hruanun, and Amporn Poyai

Thai Microelectronics Center, National Electronics and Computer Technology Center, Chacheongsao, Thailand.

\*Corresponding author, e-mail: [nithi.atthi@nectec.or.th](mailto:nithi.atthi@nectec.or.th)

---

## Abstract

This paper compares a current single-spin coating method to deposit a thick photoresist film on 14  $\mu\text{m}$  of high topology micro-structure to a multi-spin coating and a direct spray coating method. By using a single-spin coating method, the Clariant AZ-P4620 photoresist film uniformity was not so good and the remaining photoresist was not enough to block the plasma during a dry plasma etching process. When using a multi-spin coating, the multi-layers of medium viscous, Sumitomo PFI-34A, photoresist film were applied over Clariant AZ-P4620 photoresist initial layer. The photoresist film thickness has enough to block the plasma but the photoresist film peeled off during the development step due to an undercutting trouble. Then, low viscous Clariant AZ-P4999 photoresist film was coated with spray coating method. The photoresist film was thicker than a multi-spin coating method and the photoresist step coverage over the topology surface was better than the other methods. Moreover, the developed photoresist pattern has a final photoresist film thickness around 4.0  $\mu\text{m}$  on the topology surface, which is suitable for a dry etching process. It can be concluded that, the spray coating is a more suitable photoresist film coating technique on high topology surface than spin coating techniques.

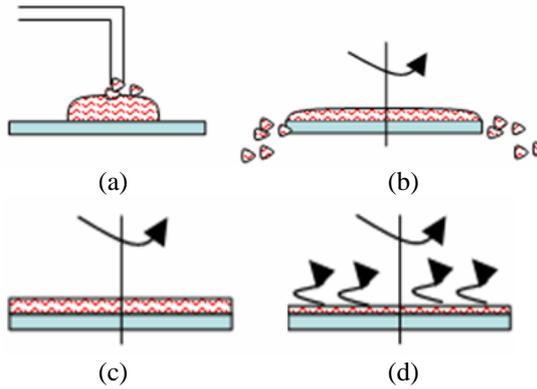
---

## Introduction

For several micro-electro mechanical systems (MEMS) applications, pattern transfer on the wafer with extensive topography requires a thick photoresist (PR), of which the film thickness is in a range of 10  $\mu\text{m}$  to 100  $\mu\text{m}$ , with a uniform PR layer over a non-planar surface. Thus, the conformal PR coating of wafers with 3D micro-structuring becomes a crucial step in the photolithography process. There is some experiment, which efforts to get a conformal coating layer by using spin coating have been reported [1]. However, this technique, even after certain modifications, presents some severe limitations for truly 3D structures. Another method is electro-deposition (ED) of PR [2]. It requires a conductive plating base layer. Therefore, electroplating of PR is restricted to the backend processing. A new alternative method, direct spray coating of PR [3-4], appears to be a promising technique as it does not require a conductive seed layer and can therefore be used at all stages of the wafer processing. In this paper, various PR coating techniques, including current single-spin coating (SS), multi-spin coating (MS) technique, and a spray coating (SC) technique, have been applied to coat a thick PR film on 14  $\mu\text{m}$  of high topology structure. The PR film thickness and film step coverage for all coating techniques have been studied.

### *Spin coating technique*

The spin coating (SC) is the prevalent method of applying PR, which is widely used in semiconductor devices manufacturing. It is intensively used to deposit uniform thin PR films to the flat substrates in photolithography process. There are four process steps in SC process, which are (1) Dispensing, (2) Spin-up, (3) Spin-off, and (4) Evaporation [5]. During a dispensing step, it can either be accomplished by flooding the entire wafer with PR solution before beginning the spinning (Static dispense), or by dispensing a smaller volume of PR solution at the center of the wafer and spinning at low speed to produce a uniform liquid layer across the wafer (Dynamic dispense). During spin-up step, the wafer is normally accelerated to the first spin speed to make the PR liquid spread off and cover the whole wafer area by using a centrifugal force. After that, the wafer is normally accelerated as fast as possible to the final spin speed. This stage is a spin-off step, which is used to control the PR film thickness. Finally, in the evaporation step, the wafer is spin at the constant final speed to make a solvent evaporate off the PR film. This stage is use to control the film uniformity. By using a spin coating technique, less than 10% of the applied PR remains on the substrate [6]. The schematic diagram of the spin coating technique has shown in Figure 1.

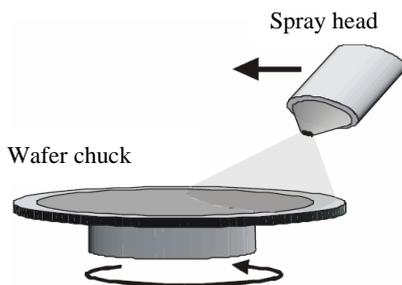


**Figure 1** The schematic view of spin coating process, (a) Dispensing, (b) Spin-up, (c) Spin-off, and (d) Evaporate.

*Spray coating technique*

A direct spray coating (SC) system has been developed and introduced by the Electronic Vision Group (EVG) in 1999. The direct spray system includes an ultrasonic spray nozzle, which generates a distribution of droplets of micrometer size. During spray coating, the wafer is rotated slowly while the swivel arm of the spray coating unit is moved across the wafer. The low spinning speed (30-60 rpm) is to minimize the centrifugal force. The rotation also allows resist coverage in all angles of the cavities [3]. Because the parts are static, no residual stresses in the coating are encountered as in spinning and the meniscus problem is significantly reduced [5].

Key parameters that influence the quality of the spray coated layer are (1) solid content of the spray solution, (2) resist dispensed volume, (3) angle of the atomizer, (4) scanning speed of atomizer, and (5) spray pressure [4]. The advantage of spray coating method is a much smaller resist amount is consumed when thick resist layers are needed. To obtain a layer of the same thickness generally a PR volume 10-15 times smaller than SS method. The disadvantage of the SC method is that the PR solution should have a viscosity less than 20 cSt. Moreover, an excessively rapid evaporation of solvents from the resist can cause "orange peel" on the substrate surface. The schematic diagram of spray coating technique is shown in Figure 2.

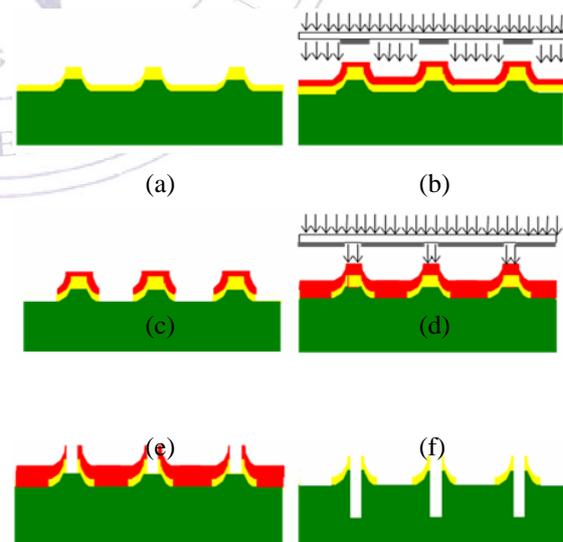


**Figure 2** The schematic view of spray coating process.

**Materials and Methods**

*Micro-needles process flow*

In this work, 6 inch p-type (100) silicon wafers were used as a substrate. The high topology surface used in the experimental was a micro-needle, which can be fabricated by using a process flow shown in Figure 3 (a) to Figure 3 (f). First, the Si wafer was coated with 2 μm of PR film and patterned by photolithography process. This PR film acts like a soft mask to protect an underneath Si surface during a plasma deep reactive ion etching (DRIE) process. The etch depth through the Si surface was 13 μm. Then, 2 μm of SiO<sub>2</sub> film was deposited on Si etched pattern surface, as a schematic shown in Figure 3 (a). Then, coated a thin PR film, which the film thickness of 2 μm, and did the patterns on PR film as the schematic shown in Figure 3 (b). After that, 2 μm of SiO<sub>2</sub> film was etched by using RIE as the schematic shown in Figure 3 (c). Then, stripped the remained PR film and coated the thick PR film, which the thickness was greater than 10 μm, on SiO<sub>2</sub> etched surface and did the patterns on thick PR as the schematic shown in Figure 3 (d). Later that, using thick PR film as a soft mask and etched through the center of SiO<sub>2</sub> opaque pattern for 150 μm depth. The fabrication structure now is shown in Figure 3 (e). Noted that, the etch selectivity between silicon (Si) and PR was 15:1. The etched SiO<sub>2</sub> structure will acts as a hard mask for Si deep trench etching process. The final micro-structure after deep trench etching process is shown in Figure 3 (f).



**Figure 3** Micro-needles fabrication process flow, (a) SiO<sub>2</sub> deposition, (b) Patterning#1, (c) SiO<sub>2</sub> etch, (d) Patterning#2, (e) Shallow trench etch, (f) Deep trench etch.

### Thick photoresist coating

This experiment is focusing on the thick PR film coating on 15  $\mu\text{m}$  of high topology surface. The high topology surface consists of 13  $\mu\text{m}$  of deep etched Si surface and covered with 2  $\mu\text{m}$  of etched  $\text{SiO}_2$  film. This PR coating process is at the process step shown in Figure 3 (d). Three kinds of PR coating methods, which are single-spin coating (SS) method, multi-spin coating (MS) and a spray coating (SC) method, have been studied.

For SS coating method, Clariantz AZ-P4620 commercial PR was coated by using TEL Mark V track coating system with a dynamic dispensing process. The PR dispensing spin speed was 500 rpm for 15 sec. After that, the wafer was accelerated at 10,000 rpm/sec to the final spin speed at 750 rpm, and span at the constant final spin speed for 10 sec. Then, PR film was baked at 100°C for 180 sec on a hot plate. The target PR film thickness was 20  $\mu\text{m}$ .

For MS coating method, it was a technique to increase a total PR film thickness beyond the limitation of the PR materials on the first layer. The topology substrate was coated with Clariantz AZ-P4620. The PR solution was dispensed for 15 sec during a wafer was spinning at 1,000 rpm. Then, the wafer was accelerated at 30,000 rpm/sec to the final spin speed at 1,500 rpm for 20 sec. Then, PR film was baked at 100°C for 180 sec on a hot plate. Then, multi-layers film stack of Sumitomo PFI-34A PR were applied over AZ-P4620 film. The PFI-34A PR was dispensed during a wafer was spinning at 1,000 rpm for 4 sec. Then, the wafer was accelerated at 30,000 rpm/sec to the final spin speed at 3,800 rpm. Hold the wafer at final spin speed for 20 sec and baked the PFI-34A PR film at 90°C for 80 sec, layer-by-layer, on a hot plate. The target film thickness of the first AZ-P4620 layer was 15 $\mu\text{m}$ , and the target film thickness of total PFI-34A film stacks was 5  $\mu\text{m}$ . This means, the total PR film thickness of AZ-P4620 PR and PFI-34A PR, which coated by MS coating method, were 20  $\mu\text{m}$ . The process conditions for SS and MS coating methods are shown in Table 1.

For SC coating method, Clariantz AZ-P4999 PR was coated on a high topology substrate. The dispensed volume of PR was 70 ml/s, spin rate of wafer was 60 rpm and the scan speed was 1,000 steps/sec across the wafer. The angle of atomizer was 45° and the spray pressure was 500 mbar. After spraying the PR layer, the wafer was baked on a hot plate at 90° C for 10 min. The target PR film thickness by SC coating method was 25  $\mu\text{m}$ . The process condition for SC coating method is shown in Table 2.

Finally, the PR film thickness and PR film coverage were investigated by Field-Emission Scanning Electron Microscope (FE-SEM), Hitachi model S4700.

**Table 1** The process conditions for SS and MS coating method.

Process step	PR coating method		
	SS	MS	
	AZ-P4620	AZ-P4620	PFI-34A
First spin speed (rpm)	500	1,000	1,000
Dispensing time (sec)	15	15	4
Acceleration (rpm/sec)	10,000	30,000	30,000
Second spin speed (rpm)	750	1,500	3,800
Second spin time (sec)	10	20	20
Soft bake temperature (°C)	100	100	90
Soft bake time (sec)	180	180	80
No. of loops	*	*	4
Target film thickness ( $\mu\text{m}$ )	20	15	5

**Table 2** The process conditions for SC coating method.

Photoresist type	AZ-P4999
Dispense volume (ml/s)	70
Wafer spin rate (rpm)	60
Scan speed (step/s)	1,000
Angle of atomizer (°)	45
PR spray pressure (mbar)	500
Soft bake temperature (°C)	90
Soft bake time (sec)	10
Target film thickness ( $\mu\text{m}$ )	25
Dispense volume (ml/s)	70

### Results and Discussion

Following by the process steps shown in Figure 3, the real micro-structure after  $\text{SiO}_2$  deposition is shown in Figure 4. First, high viscous Clariantz AZ-P4620 PR film was applied on the surface by SS method. The result in Figure 5 shows, PR film thickness (FT) on the flat surface (F-pos), pillar surface (P-pos), and the corner of the pillar (C-pos) are 12.50  $\mu\text{m}$ , 5.95  $\mu\text{m}$ , and 3.05  $\mu\text{m}$ , respectively.

After patterning, the PR film thickness coated with SS method at C-pos decreases down to 1.39  $\mu\text{m}$ , as the SEM image shown in Figure 6. The remaining PR at the C-pos was not enough to block the plasma during a dry plasma etching process because the etch selectivity between Si and PR was 15:1. So the Si substrate under a thin PR has been etched as the result is shown in Figure 7.

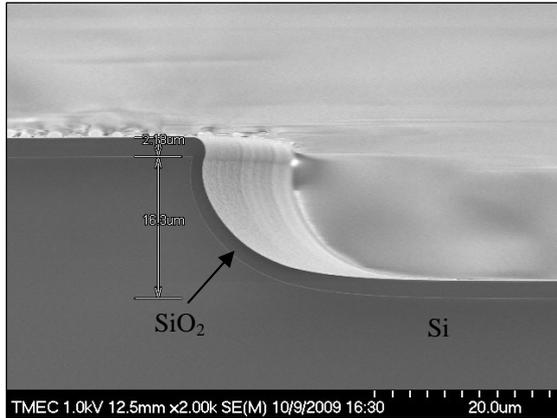


Figure 4 SEM image of SiO<sub>2</sub> film coated on Si substrate.

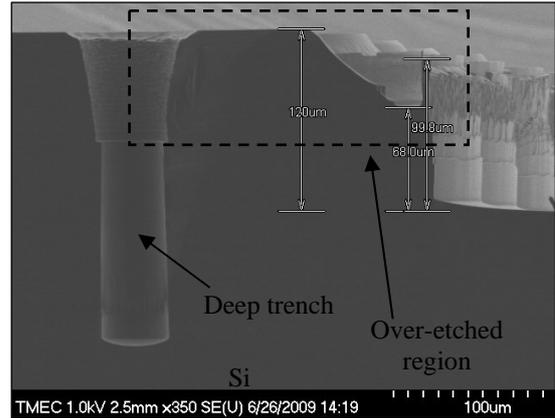


Figure 7 SEM image of a PR film coated by using SS method after etched.

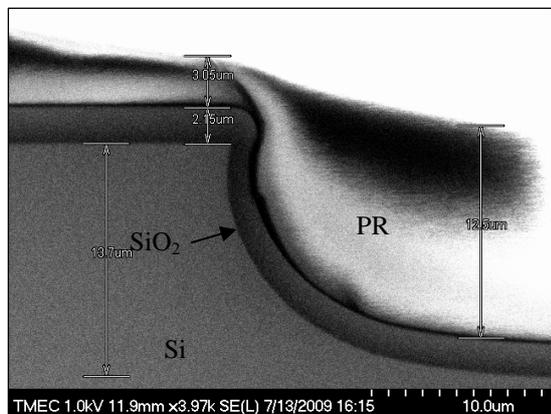


Figure 5 SEM image of a PR film coated by using SS method before exposed.

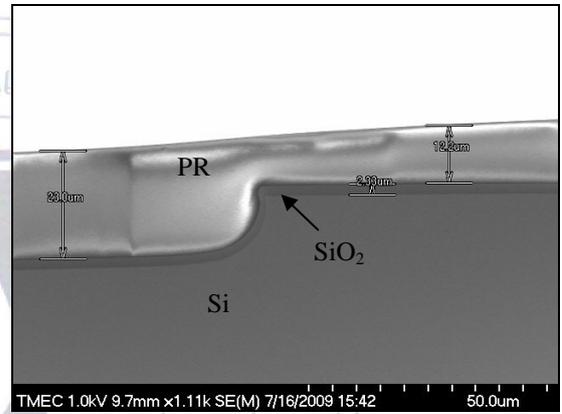


Figure 8 SEM image of a PR film coated by using MS method before exposed.

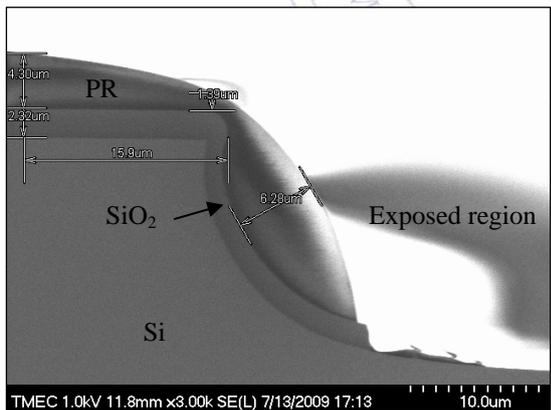


Figure 6 SEM image of a PR film coated by using SS method after developed.

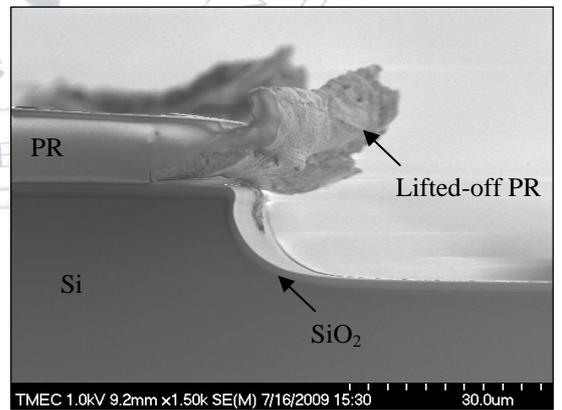


Figure 9 SEM image of a PR film coated by using MS method after developed.

For MS coating method, multi-layers of medium viscous, Sumitomo PFI-34A, PR film were applied over Clariant AZ-P4620 PR initial layer. The SEM image in Figure 8 shown that, the PR film thickness at the F-pos, P-pos, and C-pos are 23.00 μm, 10.00 μm, and 12.20 μm, respectively. The PR film thickness by the MS method was enough to block the plasma. However, the PR film stacks peeled off during the development step due to a film adhesion

and undercutting trouble as shown in Figure 9. Low viscous Clariant AZ-P4999 PR film has been applied on the surface by the SC method. Figure 10 shows the PR film thickness at F-pos, P-pos, and C-pos, which were 28.60 μm, 13.40 μm, and 12.60 μm, respectively. The PR film thickness coating with SC method was higher than MC method at C-pos and the PR step coverage and film uniformity

over the topology surface was better than the SS and MS method as the results are shown in Figure 6, Figure 8, and Figure 10, respectively. The developed pattern remains intact the PR film thickness at C-pos around 4.0µm on the topology surface, as shown in Figure 11. Moreover, the summarized of PR film thickness and film quality for various coating methods are shown in Table 3.

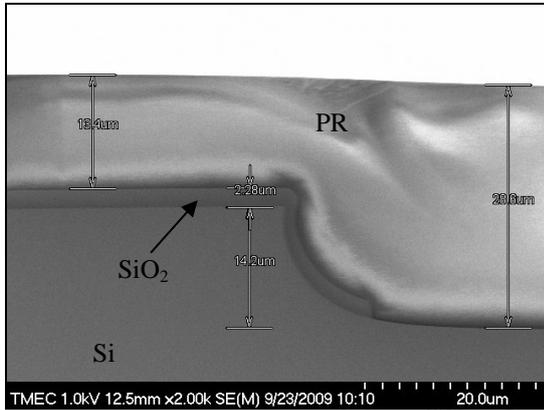


Figure 10 SEM image of a PR film coated by using SC before exposed.

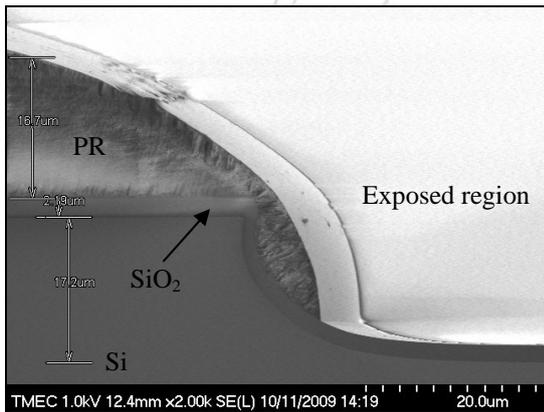


Figure 11 SEM image of a PR film coated by using SC after exposed.

Table 3 The summarized of PR film thickness and film quality for various coating methods.

	PR coating method		
	SS	MS	SC
PR type	AZ-P4620	AZ-P4620+PFI-34A	AZ-P4999
C-Pos FT (µm)	3.05	12.20	12.20
P-Pos FT (µm)	5.95	10.00	13.40
F-Pos FT (µm)	12.50	23.00	28.60
PR FT	Not enough	Enough	Enough
PR coverage	Bad	Good	Very good
PR lifted-off	No	Yes	No
Film uniformity over topology	Bad	Good	Very good

**Conclusion**

A comparison of three photoresist coating methods for MEMS structures fabrication has been presented. By using a single-spin coating, the PR film coverage was not suitable for high topology surface and the PR film thickness was not enough to block the plasma during a deep reactive ion etching process. When using a multi-spin coating, the PR film thickness and film step coverage was improved but the PR film peeled off during the development step. The results show that the spray coating is a promising technique for pattern transfer on wafers with extensive topography due to its good film thickness, good film uniformity, and good film step coverage.

**Acknowledgements**

The authors would like to thank Western Digital (Thailand) Co., Ltd. for the use of spray development machine and thanks to Nanoelectronics and MEMS laboratory, National Electronics and Computer Technology Center (NECTEC) to advice for the MEMS fabrication process step.

**References**

1. V.G. Kutchoukow, J.R. Mollinger, A. Bossche, Novel method for spinning of photoresist on wafers with through-hole, Eurosensors XIII, 256-272 (1999).
2. P. Kersten, S. Bouwstra, J.W. Petersen, Photolithography on micromachined 3D surfaces using electrodeposited photoresists, Sensor & Actuator, A51, 51-54 (1995).
3. T. Luxbacher, A. Mirza, Spray Coating for MEMS, Interconnects, and Advanced Packaging Applications, Sensors, 16, 7, 61-64 (1999).
4. N. Pham, T. Scholtes, R. Klerks, E. Boellaard, P.M. Sarro and J.N. Burghartz, Direct spray coating of photoresist—a new method for patterning 3-D structures, Eurosensors XVI, 182-185 (2002).
5. S. Wolf, R.N. Tauber: Silicon processing for VLSI era: Process technology, Vol.1, second ed., Lattice Press, California, 2000.
6. J.R. Sheat, B.W. Smith: Microlithography science and technology, Marcel Dekkar, Inc. New York, 1998.